HAPD ASIC Status

S. Nishida

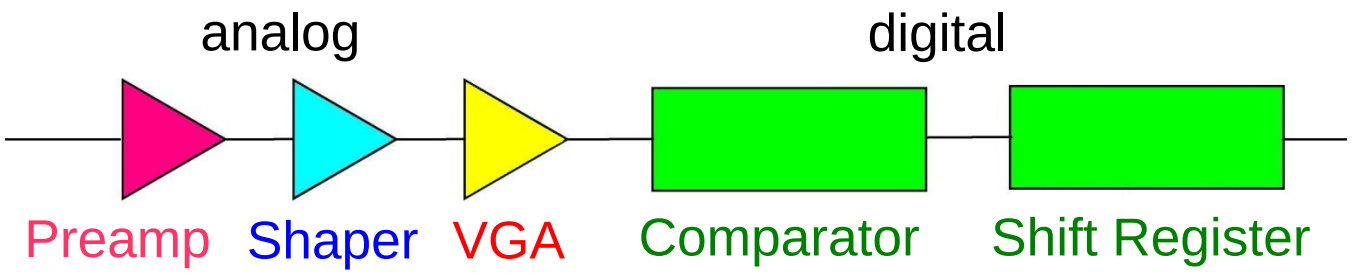
KEK

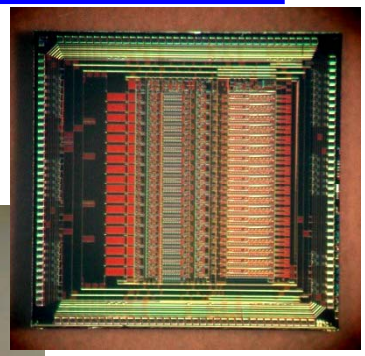
Super KEKB Meeting

Mar. 18, 2009

Readout ASIC

4 trial productions of prototype ASICs (S01-S04) at VDEC.

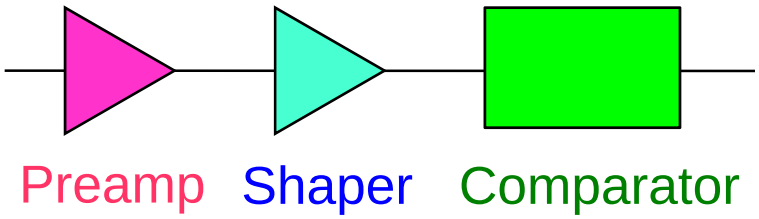




- ASIC performance O.K. (noise ~1900 p.e. @ 80pF)
- Successfully readout 1 p.e. signal from HAPDs.

Now, we are developping new prototype ASIC (SA01,SA02).

- Production at MOSIS (TSMC 0.35 μm process)
- Digital part for readout is provided with external FPGA for more flexibility to Super Belle DAQ
- More channels per chips. (target: 36ch)



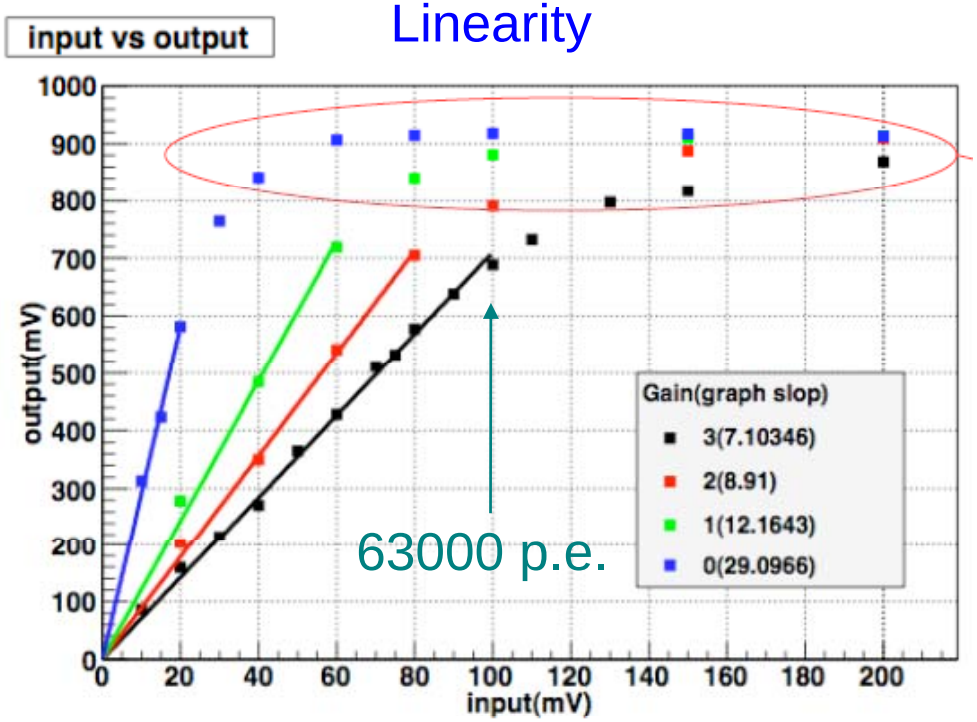
SA01

SA01 (First version of new prototype ASIC)

basic performance is O.K.

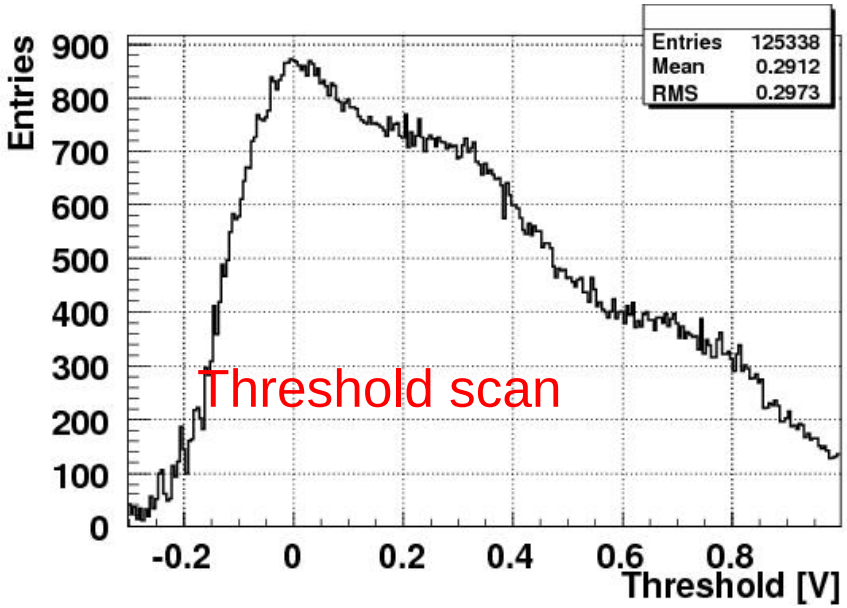
- Noise ~1200 p.e. @ 80pF (better than S04)
- Offset ajustment works fine.

Linearity



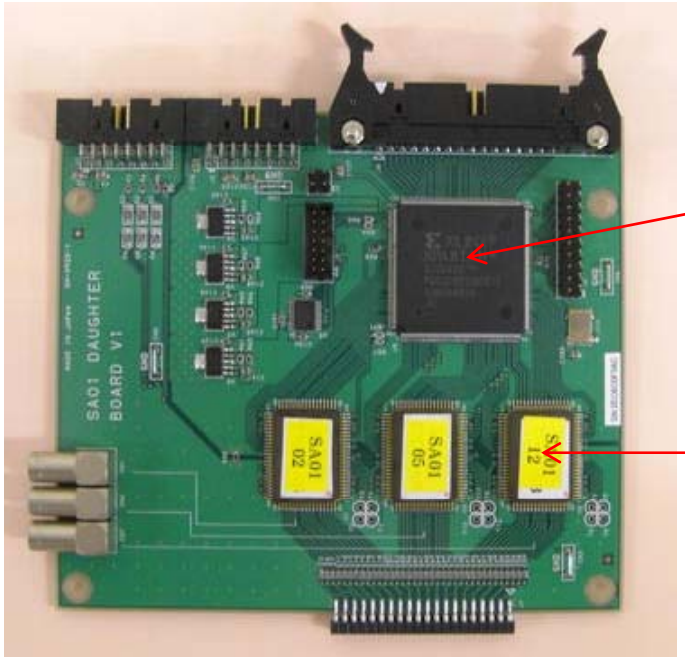
1 p.e. signal is already saturated if we apply full HV and bias voltage to HAPD.

Suffering larger noise than expected when connected with HAPD



SA01

- We have produced additonal chips ~60 chips (note: 12 chips to readout 144ch)
- New front-end test board is delivered.
  - ✓read out all of 36 ch (1/4 of HAPD) by one board.
  - ✓Confirm the scheme to put FPGA in the front-end (development of FPGA logic; effect of noise from digital part (clock etc.))
- Hopefully read out 1 HAPD in the next beam test.



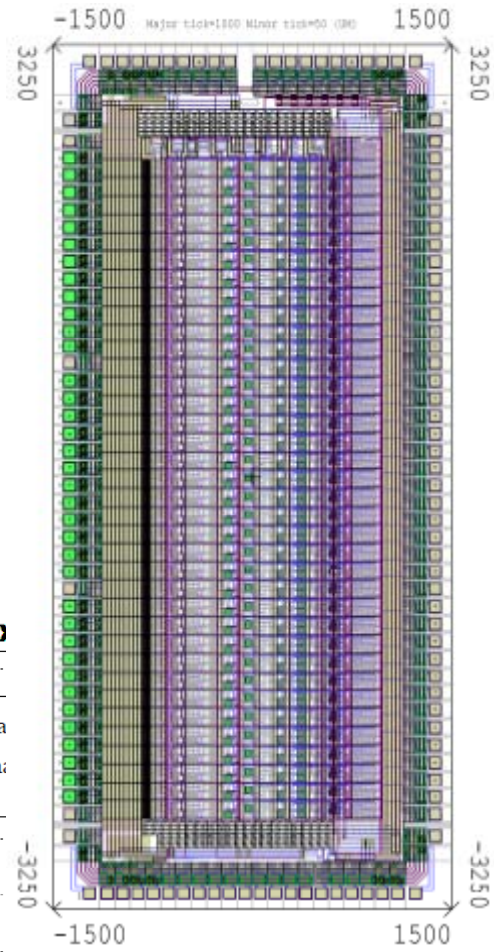
FPGA

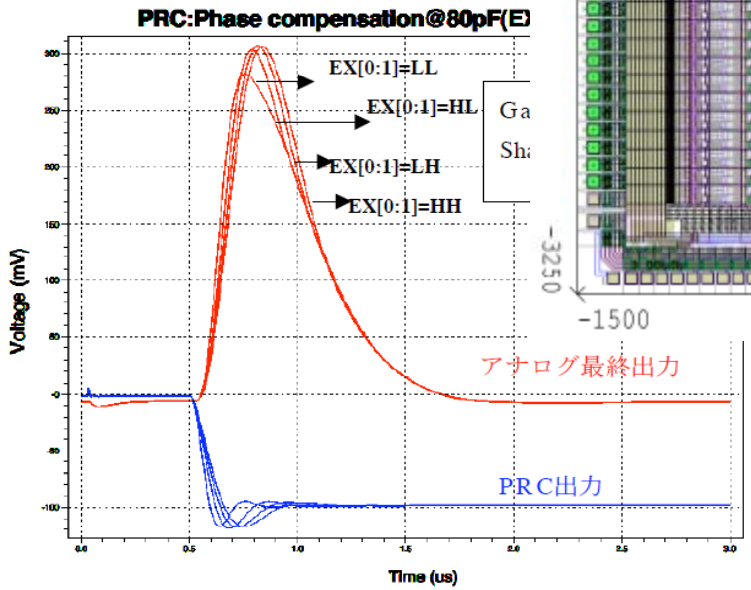
ASIC

We have just started the test

SA02

- In parallel, we are developping next version of ASIC
  - ✓36ch in one chip (i.e. read out 1 APD; need 4 ASICs for 1 HAPD)
  - ✓gain is decreased by factor 4
- Simulation O.K.
- Chip layout is done (3mm x 6mm).
- Start production in next JFY





Plan

- Test the performance.
- Develop a compact package.
- Target is a small board with 4 ASICs and 1 FPGA to readout 144ch from HAPD.